REMARKS

In response to the Official Action mailed April 4, 2003, Applicants request reconsideration. No claims are added, cancelled, or amended in this Request, so that claims 18-25 remain pending.

Telephonic Explanation

The Official Action is confusing with respect to each of the rejections. A telephonic explanation of the individual rejections was provided in a conversation with the Examiner on May 9, 2003, following previous inquiries. Although the Official Action does not explain the paragraph of 35 U.S.C. 112 relied upon in the initial rejection, the Examiner indicated that the rejection was pursuant to the first paragraph. He indicated that, to overcome the rejection, basis for the claim language cited in the rejection would have to be shown to be present in the patent application.

With regard to the prior art rejections, the Examiner acknowledged that the previous rejection of claims as unpatentable over Tsutsui (U.S. Patent 5,925,901) in view of Taguchi (U.S. Patent 5,001,108), Tozawa (JP 3-270024), and Kobayashi (JP 61-232682) was withdrawn. Taguchi is no longer relied upon in rejecting any claim. Instead of the former rejection, claims 18-25 are now rejected as unpatentable over Tsutsui in view of Tozawa and as unpatentable over Tsutsui in view of Kobayashi. It was agreed that the basis for these two rejections is not stated in detail in the Official Action.

It is with the foregoing understanding that Applicants' representative has constructed what is believed to be the prior art rejection in order to prepare the following Response.

The Rejection Pursuant to 35 U.S.C. 112, First Paragraph

The rejection pursuant to 35 U.S.C. 112, is a rejection pursuant to the first paragraph, asserting that the patent application does not support some part of the claims. Apparently the phrase asserted not be supported is the phrase describing the semiconductor substrate as being "electrically isotropic in two mutually orthogonal directions." The rejection is again respectfully traversed because it is incorrect with respect to the disclosure of the patent application and with the fundamental science of monocrystalline semiconductor materials.

With regard to the first point, asserting that the description is not supported by the patent application as filed, the Examiner's attention is directed to page 28, lines 18-22 of the patent application.

> "The reason why the gate electrode (18), etc. are bent 90° in the FET chip (10) is that, generally, the compound semiconductor materials such as gallium arsenide and the like show electrical characteristics isotopic in two directions which intersect orthogonally to each other."

While the grammar of that sentence may be questioned, the substance is not open to issue. This language provides *verbatim* support for the questioned phrase in claim 18, the only pending independent claim.

The Examiner provided definitions of the two words "anisotropic" and "isotropic". Applicants do not disagree with those definitions and the description in the patent application is not inconsistent with those definitions. The word "anisotropic" no longer appears in any pending claim because the Examiner formerly objected to that word and that word may not appear in the description of the patent application. However, those of ordinary skill in the relevant arts recognize that gallium arsenide and other compound monocrystalline semiconductor materials (as well as monocrystalline elemental semiconductor materials) are, in many characteristics, anisotropic. According to the Examiner's own definition, the term anisotropic means "exhibiting properties with different values when measured in different directions". It is notable that the definition does not state that that the property exhibited has different values in **every** different direction. The Examiner has clearly read that additional word in the definition, but that word is not present. By contrast, the word isotropic, according to the definition, means "exhibiting properties with the same value when measured along axes in *all* directions." In other words, the terms "anisotropic" and "isotropic" are not precise opposites and are not mutually exclusive. In order for those two terms to be mutually exclusive, anisotropic would be have to mean that as long as directions were different, the exhibited properties would different. However, anisotropic only means the property is different in at least two different directions.

Turning to the language questioned in the claims, that language states that the compound semiconductor substrate is "electrically isotropic into mutually orthogonal directions" and does not exclude the possibility that the substrate is anisotropic in directions that are not mutually orthogonal. The Examiner's definition of anisotropic does not prohibit a material that is anisotropic from having some directions, different from each other, along which the properties exhibited are the same. In fact, that is precisely the situation with respect to the claimed compound semiconductor substrate, the example of which provided in the patent application is GaAs. There simply is no conflict between the Examiner's definition and what is described in the patent application. Therefore, it is not understood what the Examiner's position is or how

the rejection can be made and maintained in view of the definitions provided and knowledge in the art.

With regard to knowledge in the art, if the Examiner is unfamiliar with the crystallography of monocrystalline semiconductor materials, particularly GaAs, Applicants include copies of pages 20-25 of *Modern GaAs Processing Methods* by Williams (1990). Monocrystalline materials are considered to be constructed of unit cubes of atoms. Figure 2.3 of the attached pages indicates such a unit cube for GaAs. Depending upon the crystalline orientation of a semiconductor wafer, a particular surface cutting through the unit cube may expose different densities of atoms as well as chemically different atoms.

Attention is directed to the discussion at page 23 of the attachment regarding Miller Indices used to refer to different crystallographic directions. As pointed out in the middle of that page, the (111) planes in GaAs (as well as of other monocrystalline compound semiconductor materials) may expose only Ga atoms or only As atoms, depending upon whether the A or B face is exposed. The different characteristics in different planes, which is commonly demonstrated by selective chemical etches that etch monocrystalline materials at different rates in different crystallographic directions, make materials such as GaAs anisotropic. However, these crystalline materials have various atomic symmetries so that observing the arrangement of atoms along different directions with regard, for example, to a wafer, corresponds to observing the crystalline structures along crystallographically equivalent axes. For example, considering Figure 2.3 of the attachment, it is apparent that the three mutually orthogonal directions [100], [010], and [001] are crystallographically identical. Thus, in this kind of crystalline structure, which encompasses GaAs and other materials, while the materials are anisotropic as proven by different responses to selective chemical etches, the materials have crystallographically and electrically equivalent axes that may be orthogonal to each other.

What is described in claim 18 with respected to cited phrase is simply a description of inherent characteristics of monocrystalline compound semiconductor materials that have been known and recognized for decades. There is no basis for this continuing rejection pursuant to 35 U.S.C. 112. If this issue is not to be the subject of an appeal, this rejection must be withdrawn.

The Prior Art Rejections

As noted above, it is understood that there are now two prior art rejections in which Tsutsui is the primary reference. The secondary references in the two rejections are Tozawa and Kobayashi, respectively. Pages 4-7 of the Official Action are essentially completely filled with comments based upon the prior rejection supplied, according to the Official Action, "for the sake of ready reference." It is not understood why these comments are required for ready

reference since the prior single rejection has been withdrawn and been replaced by two new rejections.

The Secondary References. At page 5 of the Official Action in his discussion of the prior rejection, the Examiner stated that Tozawa and Kobayashi each describe field effect transistor (FET) structures including adjacent channel regions having width directions essentially perpendicular to each other. It is understood that in the current rejections that Tozawa and Kobayashi are cited solely for that proposition. In other words, it is conceded by the Examiner that Tsuitsui does not describes an FET with channel regions or even source, gate, and drain electrodes, including bends. Solely for the purposes of this response, Applicants agree with the Examiner on the ground upon which Tozawa and Kobayashi are apparently cited. Stated another way, in order to establish *prima facie* obviousness of claim 18, and, therefore of any of the claims now pending, Tsutsui must supply all of the elements of the invention as defined by claim 18 with the exception of bent channel regions and bent source, gate, and drain electrodes. With regard to the somewhat tortured description in the prior Official Action, focusing on Taguchi as allegedly supplying the description of a compound semiconductor substrate that is electrically isotropic in two mutually orthogonal directions, it is noted that all three of the references now applied, Tsutsui, Tozawa, and Kobayashi concern FET structures in GaAs. Since GaAs is, as described above, a compound semiconductor substrate that is electrically isotropic at two mutually orthogonal directions, it is clear that this limitation of the claims is supplied by all of the references applied.

In the Official Action, the Examiner replied at length to the points raised in the Amendment filed January 28, 2003. Essential elements of this reply are simply wrong.

No Reference Discloses An FETWith At Least Two Active Regions. The second paragraph of claim 18 specifies that the semiconductor device claimed includes first, second, and third active regions on the first surface of the substrate. Applicants pointed out in the previous response that there is only a single active region described in the FET structure of Tsutsui. The Examiner disagreed. The Examiner's position is incorrect based upon the express disclosure of Tsutsui.

In the Official Action, the Examiner reproduced Figure 1 of Tsutsui and part of the description appearing in column 1 of Tsutsui and pertaining to that figure. The description clearly states that what is shown in Tsutsui's Figure 1 is a structure including four unit cells. From that statement, the Examiner concludes that there are four active regions in the figure.

However, the Examiner's position is without any support in Figure 1 of Tsutsui or the description of that figure. In fact, the lines of Tsutsui reproduced in the Official Action refer to the active region in the singular, not plural. Moreover, no description within Tsutsui ever refers to more than one active region.[1]

An inspection of Figure 1 of Tsutsui shows a broken line indicated as the boundary of the active region 2. The active region 2 extends horizontally across Figure 1. This area is totally uninterrupted, demonstrating very clearly that there is only a single active region in the structure shown in that Figure 1 of Tsutsui. The same single active region 2 is illustrated in Figure 4 of Tsutsui and likewise described in the singular throughout the disclosure of Tsutsui.

Embodiments of what Tsutsui considers as his invention are illustrated in Figures 7 and 11 of that patent and show identical single active regions 2, described in Tsutsui in the singular. It is clear that in the regions separating the unit cells of Tsutsui from each other in Figures 7 and 11, that the connecting lines of the active region 2 are obscured by other overlying elements. However, there is no basis whatsoever in Tsutsui for concluding that there are multiple active regions like the first, second, and third active regions of the claimed structure. (The cross-sectional views in Figures 2, 5, 8, and 12 of Tsutsui are taken at locations that do not reveal any further information concerning the structure of the active region.)

At page 9 of the Official Action, the Examiner reproduced part of the text of Tsutsui, from column 3, directed to Figure 7 of that patent. The reproduced passage refers to the active region 2 at two different locations, each time in the singular. At the conclusion of the reproduction of the passage from Tsutsui, the Examiner concluded, without explaining the basis for the conclusion, that this passage describes multiple active regions. The passage does not include any such description. Further, the Examiner's reference to a region 16 is not understood since no reference number 16 used in Tsutsui.

Applicants reiterate that *prima facie* obviousness cannot be established with respect to any pending claim through the use of Tsutsui as the primary reference because Tsutsui does not describe a semiconductor device structure including first, second, and third active regions separated from each on the surface of a compound semiconductor substrate. The Examiner's contrary view finds no particle of support in Tsutsui. In addition, Tsutsui is lacking other important elements of the invention as defined by claim 18.

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[1] After many searches during the prosecution of this patent application, the undersigned first located on May 19, 2003, the Japanese patent application on which Tsutsui is based, published as JP-9-45706. Tsutsui includes no priority claim making the search difficult. A copy of that publication and a computer-generated translation of it from the JPO are attached. The description there fully supports Applicants' position, not the view of the Examiner.

There Are No First And Second Insulating Regions In Tsutsui. In the structure of claim 18, the first and second active regions are separated by a first insulating region. The second and third active regions are separated by a second insulating region. Contrary to the Examiner's assertion, nothing similar is described by Tsutsui.

In taking the contrary position, the Examiner reproduced a passage from column 4 of Tsutsui at page 9 of the Official Action. That passage refers to the single active region 2 of Tsutsui as being surrounded by an electrically insulating region formed by ion implantation. It is apparent from inspecting the relevant figures of Tsutsui, Figures 1, 4, 7, and 11, that the single active region 2 is surrounded by an electrically insulating region. It is unknown how that single insulating region, which is not even given a reference number in Tsutsui, can be considered by the Examiner to constitute two electrically insulating regions that separate respective pairs of active regions from each other.

It is presumed, referring to, for example, Figure 7 of Tsutsui that the Examiner is concluding that the active region 2 is separated between each of the four indicated cells by an insulating region that extends vertically in that figure between neighboring cells. There is no basis in the description of Tsutsui for that interpretation. The Examiner is importing knowledge of the invention and using that knowledge to give an unwarranted and incorrect interpretation to Figure 7 (and other figures) of Tsutsui. If there were separate active regions 2 in each cell, Tsutsui would include such a disclosure. If there were insulating regions between the respective cells of Tsutsui, electrically isolating each cell from each other cell, Tsutsui would describe the insulating regions. In the absence of any such express description, the position taken by the Examiner at page 9 of the Official Action cannot be reasonably maintained. The absence of this additional important element of the claims further demonstrates that *prima facie* obviousness cannot be established by modifying Tsutsui with either of Tozawa and Kobayashi.

Tsutsui Does Not Provide One FET On Multiple Active Regions. There are still more elements of the structure defined by the pending claims that are not present in any reference applied in rejecting the claims. For example, the claimed structure includes first and second semiconductor elements. *Each* of those first and second semiconductor elements is disposed on the first, second, and third channel regions. Because those channel regions extend across the substrate, the two semiconductor elements are disposed, at different locations, on parts of the same first, second, and third channel regions. If the Examiner's interpretation of Tsutsui were accepted, for the sake of argument, asserting that there are plural active regions in Tsutsui, Tsutsui would still not meet or even suggest the invention claimed.

Adopting, for example, with respect to Figure 7 of Tsutsui, the Examiner's interpretation, each unit cell 3 includes a totally independent active region 2. There is no semiconductor element, i.e., FET, disposed on more than one of these unit cells in any structure described by Tsutsui. Rather, each unit cell is, according to the Examiner's interpretation, completely independent. If it is accepted, for the sake of argument, that each unit cell is separated by an insulating region, how is it possible that the first semiconductor element shown in the leftmost cell of Figure 7 of Tsutsui could also be disposed on the active regions of the next successive unit cell, moving to the right in Figure 7? In other words, if Applicants accept the Examiner's interpretation of Tsutsui, although that interpretation is incorrect, the interpretation still fails to establish *prima facie* obviousness of any pending claim because neither Tsutsui nor Tazawa nor Kobayashi describes a structure with three active regions, mutually separated by insulating regions, in which two different field effect transistors are disposed on all three of the active regions. The rejection cannot be reasonably maintained as to this or any of the two previously discussed points.

No Reference Discloses Gate Bends On Separate Insulating Regions. A particularly important feature of the invention, not addressed in any of the Official Actions, is described in the final paragraph of claim 18. As described in the final four lines of that final paragraph, the first insulating region is under the first and third bending positions of the first and second gate electrodes, i.e., of the first *and* second semiconductor elements, and the second insulating region is under the second and fourth bending positions of the first and second gate electrodes, i.e., of the first and second semiconductor elements. This arrangement is clearly shown in the embodiment illustrated in Figure 5 of the patent application with three active regions 16, two insulating regions 14a, and multiple FET units 44, each with doubly bent electrodes. That embodiment further makes clear the relative arrangements of the first, second, and third active regions as well as of the first and second insulating regions.

No matter how the structure described in Tsutsui is stretched, twisted, or jiggered, there is no possible situation in which any gate electrode, Gf, would ever overlie the insulating region between two unit cells. Moreover, to meet claim 18, such an arrangement would have to exist with respect to gate electrodes of two different field effect transistors of two different unit cells to support the rejection. If the Examiner's interpretation of Tsutsui's Figures 1, 4, 7, and 11 were correct, then an important element of the depicted structures would be the mutual isolation of the individual side-by-side cells by the electrically insulating regions. Tsutsi never suggests extending electrodes across those insulating regions. There is simply no possibility that any gate

electrode would overlie those distinct and mutually isolated regions in Tsutsui as in the claimed invention. On this ground also, the rejection cannot be reasonably maintained.

Summary

Because of the four independent differences, discussed above, between the structure expressly defined by claims 18-25 and Tsutsui, even as modified by either of Tozawa and Kobayashi, there is no possibility of demonstrating *prima facie* obviousness of any pending claim with those references. Upon reconsideration, the rejection should be withdrawn and claims 18-25 allowed, promptly concluding this protracted prosecution without the necessity of an appeal.

Respectfully submitted,

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